

Figure 1a: Single-Thread Processor. This figure shows a sequence of 40 machine cycles for a single-thread processor. The cycles are labeled 1 through 40, and the processor state is shown for each cycle. The states are: PC (Program Counter), FETCH, DECODE, OPERAND, EXECUTE, ADDRESS, MEM (Memory), MEM (Memory), MEM (Memory), and WRITEBACK. The states are shown in a sequence of 40 cycles, with the states for each cycle being: PC (A), FETCH (A), DECODE (A), OPERAND (A), EXECUTE (A), ADDRESS (A), MEM (A), MEM (A), MEM (A), and WRITEBACK (A). The states are shown in a sequence of 40 cycles, with the states for each cycle being: PC (A), FETCH (A), DECODE (A), OPERAND (A), EXECUTE (A), ADDRESS (A), MEM (A), MEM (A), MEM (A), and WRITEBACK (A).

Single-Thread Processor

machine cycle	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40		
PC	A	B	C	D	E	E	E	E	E	E	F	F	F	F	F	F	F	F	G	G	G	H	H	H	H	H	H	H	I	I	I	I	I	I	J	J	J	J	J	J		
FETCH		A	B	C	D	D	D	D	D	D	D	D	D	D	D	D	E	E	E	F	F	F	F	F	F	F	F	F	G	H	H	H	H	I	I	I	I	I	I	I		
DECODE			A	B	C	C	C	C	C	C	C	D	D	D	D	D	E	E	E	E	E	F	F	F	F	F	F	F	F	G	G	G	H	H	H	H	H	H	H	H	H	
OPERAND				A	B	B	B	B	B	B	B	C	C	C	C	C	D	D	D	D	D	E	E	E	E	E	E	E	E	F	F	F	F	F	G	G	G	G	G	G		
EXECUTE					A							B					C						D																			
ADDRESS						A							B					C						D						E						F						
MEM							A						B						C						D						E					F						
MEM								A						B						C												E						F				
MEM									A						B						C																					
WRITEBACK										A						B						C																				
memory in use							1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 1a

Single-Thread Processor with Data Cache

machine cycle	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	
PC	A	B	C	D	E	E	E	F	F	F	G	G	G	H	H	H	I	I	I	J	J	J	K	K	K	L	L	L	L	M	M	M	N	N	N	O	O	P	P	P	
FETCH		A	B	C	D	D	D	E	E	E	F	F	F	G	G	G	H	H	H	I	I	J	J	J	K	K	K	L	L	L	M	M	M	N	N	N	O	O	O	O	
DECODE			A	B	C	C	C	D	D	D	E	E	E	F	F	F	G	G	G	H	H	I	I	J	J	J	K	K	K	L	L	L	M	M	M	N	N	N	O	O	O
OPERAND			A	B	B	B	B	C	C	C	D	D	D	D	E	E	E	F	F	F	G	G	H	H	H	I	I	I	J	J	J	K	K	K	L	L	L	M	M	M	M
EXECUTE				A				B			C		D		D		E	E		F		G		G		H							J		K						
ADDRESS					A				B		C				D		E				F				G			H			I		J								
WRITEBACK						A				B			C			D			E			F											I		J		K				

Figure 1b

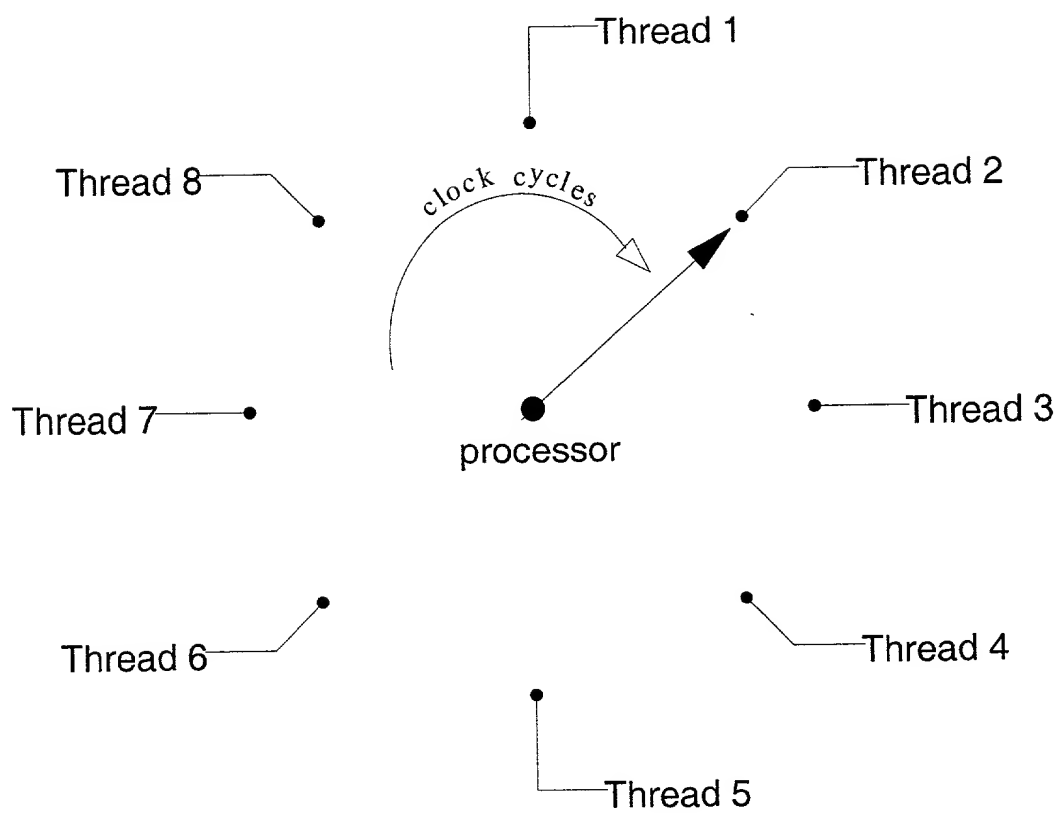


Figure 2

## Four-Thread Processor

active thread	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4
PC	1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C	1D	2D	3D	4D	1E	2E	3E	4E
FETCH	1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C	1D	2D	3D	4D	1E	2E	3E	4E
DECODE	1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C	1D	2D	3D	4D	1E	2E	3E	4E
OPERAND	1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C	1D	2D	3D	4D	1E	2E	3E	4E
EXECUTE	1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C	1D	2D	3D	4D	1E	2E	3E	4E
ADDRESS	1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C	1D	2D	3D	4D	1E	2E	3E	4E
MEM	1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C	1D	2D	3D	4D	1E	2E	3E	4E
MEM	1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C	1D	2D	3D	4D	1E	2E	3E	4E
MEM	1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C	1D	2D	3D	4D	1E	2E	3E	4E
WRITEBACK	1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C	1D	2D	3D	4D	1E	2E	3E	4E
memory in use	1	1	1	1	2	2	2	2	3	3	3	3	4	4	4	4	1	1	1	1

Figure 3a

## Four-Thread Processor with Banked Memory

active thread	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4
PC	1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C	1D	2D	3D	4D	1E	2E	3E	4E
FETCH	1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C	1D	2D	3D	4D	1E	2E	3E	4E
DECODE	1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C	1D	2D	3D	4D	1E	2E	3E	4E
OPERAND	1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C	1D	2D	3D	4D	1E	2E	3E	4E
EXECUTE	1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C	1D	2D	3D	4D	1E	2E	3E	4E
ADDRESS	1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C	1D	2D	3D	4D	1E	2E	3E	4E
MEM	1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C	1D	2D	3D	4D	1E	2E	3E	4E
MEM	1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C	1D	2D	3D	4D	1E	2E	3E	4E
MEM	1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C	1D	2D	3D	4D	1E	2E	3E	4E
WRITEBACK	1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C	1D	2D	3D	4D	1E	2E	3E	4E
memory1 in use	1	1	1	1	3	3	3	3	1	1	1	1	3	3	3	3	1	1	1	1
memory2 in use	2	2	2	2	4	4	4	4	2	2	2	2	4	4	4	4	2	2	2	2

Figure 3b

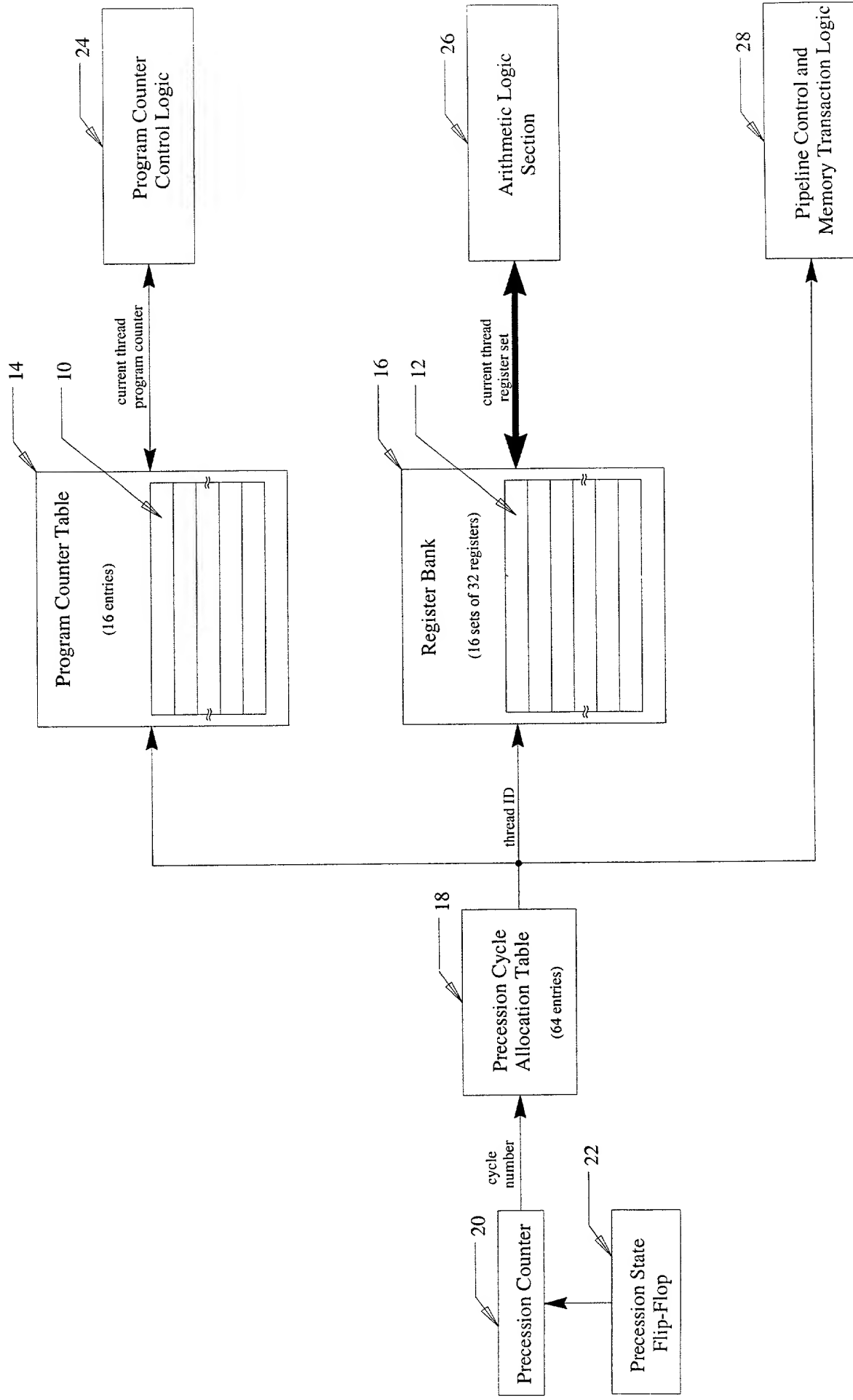


Figure 4

# Cycle Allocation Table

- 1
- 2
- 3
- 4
- 5
- 6
- 7
- 8
- 9
- 10
- 11
- 12
- 13
- 14
- 15
- 16
- 1
- 2
- 3
- 4
- 5
- 6
- 7
- 8
- 9
- 10
- 11
- 12
- 13
- 14
- 15
- 16
- ...
- ...

commutator

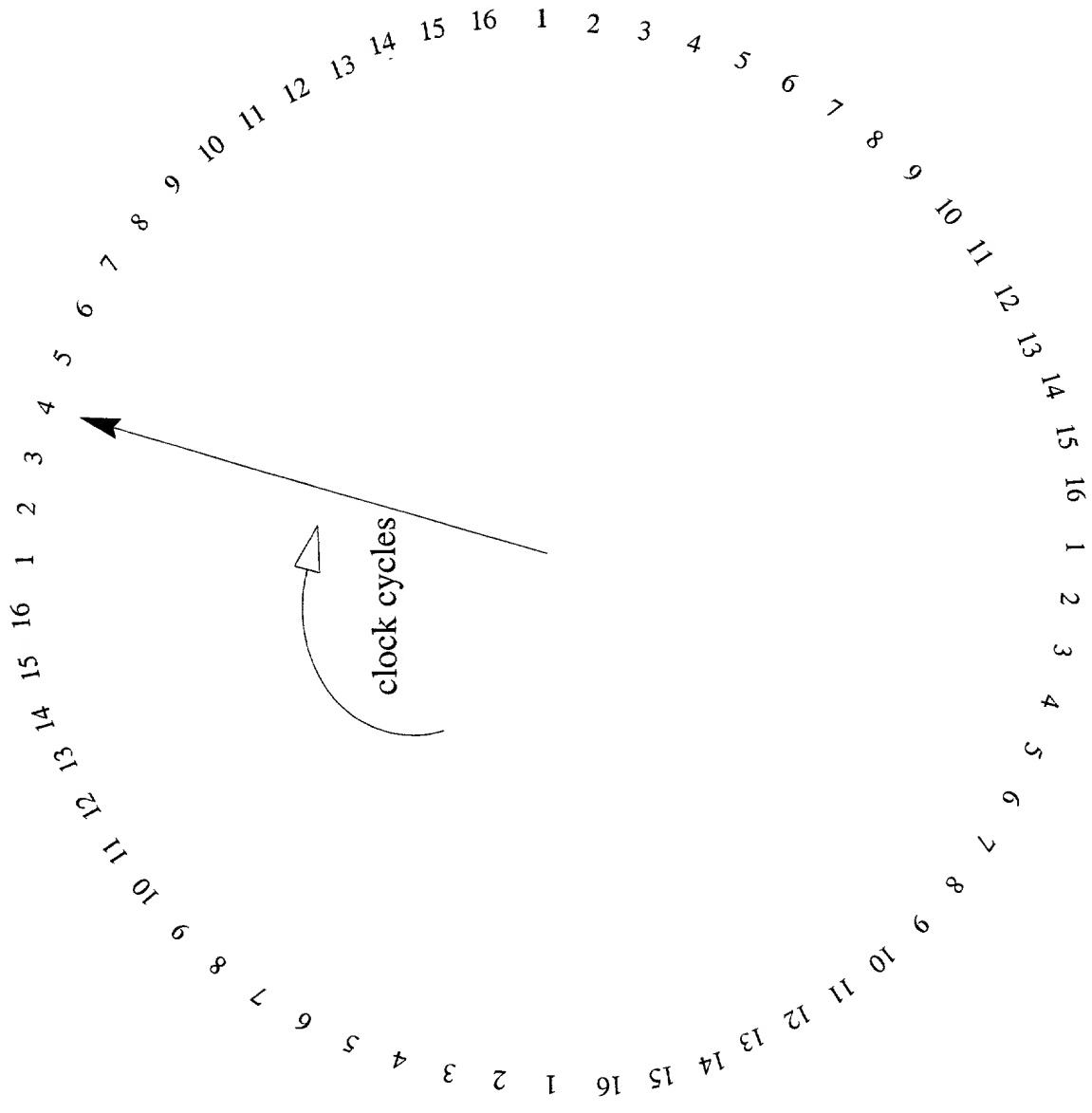


Figure 5

Figure 6: Cycle Allocation Table

# Cycle Allocation Table

commutator

